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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/256,265	02/23/1999	DAH-BIN KAO	16405-311	9612

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EXAMINER
DIAZ, JOSE R

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/13/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/256,265	KAO ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,8-10,16 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8-10,16 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

➢ A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 18, 2001 has been entered.

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

➢ Claims 1 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Middelhoek et al. (US Patent No. 5,216,269) in view of Yoshimi (JP 4-241468).

Regarding claims 1 and 16, Middelhoek et al. teach a substrate; a defined channel region; a floating gate (11) disposed over said channel region separated therefrom by a first insulating layer (21); a control gate (12) placed on one side of said floating gate (11) separated therefrom by a second insulating layer (22); a erase gate (14) placed on second side of said floating gate (11) separated therefrom by said second insulating layer (22); a drain region (6) disposed on a first side of said floating gate (11); and a source region (5) disposed on a second side of said floating gate (11) (see Figure 10). However, Middelhoek et al. do not teach the limitation of providing a control gate having a first portion disposed over a portion of the substrate and being separated by said second insulating layer, a second portion formed over a first one of said sidewalls of said floating gate and a third portion formed over at least a portion of said top surface of said floating gate, said second portion having a surface substantially parallel to and opposing said first sidewalls. Yoshimi teaches that is well known in the art to form an erase gate (15) and a control gate (CG) on each sidewall of the floating gate (FG), wherein the control gate covers top portion and a sidewall of the floating gate, and portion of the substrate (see Figs. 7a-8c). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Middelhoek et al. to include a control gate which extends over top portion and a sidewall of the floating gate, and portion of the substrate. The ordinary artisan would

have been motivated to modify Middelhoek et al. in the manner described above for at least the purpose of forming an EEPROM device.

➢ Claims 2, 8-10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Middelhoek et al. (US Patent No. 5,216,269) in view of Yoshimi (JP 4-241468), and further in view of Chang (US Patent No. 6,125,060).

Regarding claim 8-9, Middelhoek et al. teach a substrate; a defined channel region; a floating gate (11) disposed over said channel region separated therefrom by a first insulating layer (21); a control gate (12) placed on one side of said floating gate (11) separated therefrom by a second insulating layer (22); a erase gate (14) placed on second side of said floating gate (11) separated therefrom by said second insulating layer (22); a drain region (6) disposed on a first side of said floating gate (11); and a source region (5) disposed on a second side of said floating gate (11) (Figure 10). However, Middelhoek et al. do not teach the limitation of providing a control gate having a first portion disposed over a portion of the substrate and being separated by said second insulating layer, a second portion formed over a first one of said sidewalls of said floating gate and a third portion formed over at least a portion of said top surface of said floating gate, said second portion having a surface substantially parallel to and opposing said first sidewalls. Yoshimi teaches that is well known in the art to form an erase gate (15) and a control gate (CG) on each sidewall of the floating gate (FG), wherein the control gate covers top portion and a sidewall of the floating gate, and portion of the substrate (see Figs. 7a-8c). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify

Middelhoek et al. to include a control gate which extends over top portion and a sidewall of the floating gate, and portion of the substrate. The ordinary artisan would have been motivated to modify Middelhoek et al. in the manner described above for at least the purpose of forming an EEPROM device.

In addition, a further different between the claimed invention and the reference is the limitation of how the control gate, erase gate, source and drain are connected in the device. Chang teaches a memory array (214) comprising a plurality of memory cells each having a floating gate (103), an erase gate (122), a control gate (101), a source region (105), and a drain region (108) (Figure 1f) comprising: a plurality of rows and columns of interconnected memory cells wherein the control gates (CG(i)) of memory cells in the same row are connected by a common word-line (201); the erase gates (EG(m)) of memory cells in the same row are connected by a common erase-line (207); the source regions (Source(m)) of memory cells in the same row are connected by a common source-line (205); the drain regions (208) of memory cells in the same row are connected by a common drain-line (BL (i)); and control circuit connecting to circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array (Figure 3). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to further modify Middelhoek et al. to include a plurality of rows and columns of interconnected memory cells wherein the control gates of memory cells in the same row are connected by a common word-line; the erase gates of memory cells in the same row are connected by a common erase-line; the source regions of memory cells in the

same row are connected by a common source-line; the drain regions of memory cells in the same row are connected by a common drain-line; and control circuit connecting to circuit connecting to said word-lines, erase lines, source lines and drain lines for operating one or more memory cells of said memory array. The ordinary artisan would have been motivated to further modify Middelhoek et al. in the manner described above for at least the purpose of manufacturing a memory device having low currents for both program and erase operations.

Regarding claims 2, 10 and 17, a further different between the claimed invention and the reference is the limitation wherein an erase gate overlaps a floating gate and a control gate. Chang teaches that is well known in the art to provide an erase gate (122) that overlaps the floating gate (103) and said control gate (101) (Figure 1f). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to further modify Middelhoek et al. to include an erase gate overlaping the floating gate and the control gate. The ordinary artisan would have been motivated to further modify Middelhoek et al. in the manner described above for at least the purpose of manufacturing a memory device having low currents for both program and erase operations.

- Claims 1 and 16 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Van Houdt et al. (US Patent No. 5,583,810).

Regarding claims 1 and 16, Van Houdt et al. teach a substrate (11); a defined channel region; a floating gate (FG) disposed over said channel region separated

therefrom by a first insulating layer (consider layer between the floating gate and the substrate); a control gate (CG) placed on one side of said floating gate (FG) separated therefrom by a second insulating layer (consider layer that is between the FG and CG); a erase gate (PG) placed on second side of said floating gate (FG) separated therefrom by said second insulating layer (consider layer that is between the FG and PG); a drain region (D) disposed on a first side of said floating gate (FG); and a source region (S) disposed on a second side of said floating gate (FG) (see Figures 1-3).

Response to Arguments

- Applicant's arguments with respect to claims 1-2, 8-10, and 16-17 have been considered but are moot in view of the new ground(s) of rejection.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00 - 5:00 Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
March 7, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800